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IEEE CNF IEEE Conference Proceeding

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IEEE STD IEEE Standard

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- ☐ 1. **On the use of VHDL-based behavioral synthesis for telecom ASIC design**
Genoe, M.; Vanoostende, P.; Van Wauwe, G.;
System Synthesis, 1995., Proceedings of the Eighth International Symposium ·
13-15 Sept. 1995 Page(s):96 - 101
Digital Object Identifier 10.1109/ISSS.1995.520619
[AbstractPlus](#) | Full Text: [PDF](#)(572 KB) IEEE CNF
- ☐ 2. **A methodology for verifying memory access protocols in behavioral synt**
Koch, G.; Taewhan Kim; Genevriere, R.;
Computer Aided Design, 2000. ICCAD-2000. IEEE/ACM International Confere:
5-9 Nov. 2000 Page(s):33 - 38
Digital Object Identifier 10.1109/ICCAD.2000.896447
[AbstractPlus](#) | Full Text: [PDF](#)(552 KB) IEEE CNF
- ☐ 3. **Matisse: an architectural design tool for commodity ICs**
Kucukcakar, K.; Chih-Tung Chen; Jie Gong; Philipsen, W.; Tkacik, T.E.;
Design & Test of Computers, IEEE
Volume 15, Issue 2, April-June 1998 Page(s):22 - 33
Digital Object Identifier 10.1109/54.679205
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(188 KB) IEEE JNL
- ☐ 4. **Behavioral synthesis of fault secure controller/datapaths based on aliasi**
analysis
Lakshminarayana, G.; Raghunathan, A.; Jha, N.K.;
Computers, IEEE Transactions on
Volume 49, Issue 9, Sept. 2000 Page(s):865 - 885
Digital Object Identifier 10.1109/12.869319
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(532 KB) IEEE JNL
- ☐ 5. **Using estimates from behavioral synthesis tools in compiler-directed des**
exploration
So, B.; Diniz, P.C.; Hall, M.W.;
Design Automation Conference, 2003. Proceedings
2-6 June 2003 Page(s):514 - 519
[AbstractPlus](#) | Full Text: [PDF](#)(777 KB) IEEE CNF
- ☐ 6. **Rethinking behavioral synthesis for a better integration within existing de**

*Behavioral Design
Synthesized to
reprog. logic /ASIC*

Cesario, W.O.; Jerraya, A.A.; Sugar, Z.; Moussa, I.;
Computer Design, 2000. Proceedings. 2000 International Conference on
17-20 Sept. 2000 Page(s):513 - 518
Digital Object Identifier 10.1109/ICCD.2000.878330
[AbstractPlus](#) | Full Text: [PDF\(532 KB\)](#) IEEE CNF

- ☐ **7. Architectural simulation in the context of behavioral synthesis**
Jemai, A.; Kission, P.; Jerraya, A.A.;
Design, Automation and Test in Europe, 1998., Proceedings
23-26 Feb. 1998 Page(s):590 - 595
Digital Object Identifier 10.1109/DATE.1998.655918
[AbstractPlus](#) | Full Text: [PDF\(116 KB\)](#) IEEE CNF

- ☐ **8. Behavioral synthesis**
Camposano, R.;
Design Automation Conference Proceedings 1996, 33rd
3-7 June 1996 Page(s):33 - 34
[AbstractPlus](#) | Full Text: [PDF\(204 KB\)](#) IEEE CNF

- ☐ **9. Behavioral synthesis of fault secure controller/datapaths using aliasing p
analysis**
Lakshminarayana, G.; Raghunathan, A.; Jha, N.k.;
Fault Tolerant Computing, 1996., Proceedings of Annual Symposium on
25-27 June 1996 Page(s):336 - 345
Digital Object Identifier 10.1109/FTCS.1996.534618
[AbstractPlus](#) | Full Text: [PDF\(1108 KB\)](#) IEEE CNF

- ☐ **10. Optimisation efficiency in behavioural synthesis**
Baker, K.R.; Brown, A.D.; Currie, A.J.;
Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G
Devices and Systems]
Volume 141, Issue 5, Oct. 1994 Page(s):399 - 406
[AbstractPlus](#) | Full Text: [PDF\(512 KB\)](#) IEE JNL

- ☐ **11. Behavioural synthesis support system for undergraduate teaching**
Ainscough, J.; Southall, D.M.; Oakey, S.; Goodwin, A.;
Circuits, Devices and Systems, IEE Proceedings G
Volume 139, Issue 2, April 1992 Page(s):149 - 153
[AbstractPlus](#) | Full Text: [PDF\(352 KB\)](#) IEE JNL

- ☐ **12. Embedded architectural simulation within behavioral synthesis environr**
Jemai, A.; Kission, P.; Jerraya, A.A.;
Design Automation Conference 1997. Proceedings of the ASP-DAC '97. Asia ;
28-31 Jan. 1997 Page(s):227 - 232
Digital Object Identifier 10.1109/ASPDAC.1997.600127
[AbstractPlus](#) | Full Text: [PDF\(632 KB\)](#) IEEE CNF

- ☐ **13. Behavioral synthesis for easy testability in data path allocation**
Lee, T.C.; Wolf, W.F.; Jha, N.K.; Acken, J.M.;
Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proce-
1992 International Conference on
11-14 Oct. 1992 Page(s):29 - 32
Digital Object Identifier 10.1109/ICCD.1992.276212
[AbstractPlus](#) | Full Text: [PDF\(352 KB\)](#) IEEE CNF

- ☐ **14. Optimisation in behavioural synthesis using hierarchical expansion: moc**
Williams, A.C.; Brown, A.D.; Baidas, Z.;
Computers and Digital Techniques, IEE Proceedings-

Volume 148, Issue 1, Jan 2001 Page(s):31 - 43
Digital Object Identifier 10.1049/ip-cdt:20010208
[AbstractPlus](#) | Full Text: [PDF](#)(996 KB) IEE JNL

- ☐ **15. Towards behavioral synthesis of asynchronous circuits - an implemental targeting syntax directed compilation**
Nielsen, S.F.; Sparso, J.; Madsen, J.;
Digital System Design, 2004. DSD 2004. Euromicro Symposium on
31 Aug.-3 Sept. 2004 Page(s):298 - 305
Digital Object Identifier 10.1109/DSD.2004.1333290
[AbstractPlus](#) | Full Text: [PDF](#)(371 KB) IEEE CNF

- ☐ **16. Behavioral synthesis of datapaths with low leakage power**
Gopalakrishnan, C.; Katkoori, S.;
Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on
Volume 4, 26-29 May 2002 Page(s):IV-699 - IV-702 vol.4
Digital Object Identifier 10.1109/ISCAS.2002.1010552
[AbstractPlus](#) | Full Text: [PDF](#)(370 KB) IEEE CNF

- ☐ **17. A top-down interactive behavioral synthesis environment**
Poulakis, I.P.; Economakos, P.; Economakos, G.; Panagopoulos, I.; Papakons
Electronics, Circuits and Systems, 2000. ICECS 2000. The 7th IEEE Internatic
on
Volume 1, 17-20 Dec. 2000 Page(s):516 - 519 vol.1
Digital Object Identifier 10.1109/ICECS.2000.911591
[AbstractPlus](#) | Full Text: [PDF](#)(396 KB) IEEE CNF

- ☐ **18. An approach to behavioral synthesis for loop-based BIST**
Xiaowei Li; Cheung, P.Y.S.;
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE Interna
on
Volume 6, 30 May-2 June 1999 Page(s):374 - 377 vol.6
Digital Object Identifier 10.1109/ISCAS.1999.780173
[AbstractPlus](#) | Full Text: [PDF](#)(348 KB) IEEE CNF

- ☐ **19. Design for hierarchical testability of RTL circuits obtained by behavioral**
Ghosh, I.; Raghunathan, A.; Jha, N.K.;
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proce
IEEE International Conference on
2-4 Oct. 1995 Page(s):173 - 179
Digital Object Identifier 10.1109/ICCD.1995.528807
[AbstractPlus](#) | Full Text: [PDF](#)(772 KB) IEEE CNF

- ☐ **20. Behavioral synthesis for low power**
Raghunathan, A.; Jha, N.K.;
Computer Design: VLSI in Computers and Processors, 1994. ICCD '94. Proce
International Conference on
10-12 Oct. 1994 Page(s):318 - 322
Digital Object Identifier 10.1109/ICCD.1994.331915
[AbstractPlus](#) | Full Text: [PDF](#)(492 KB) IEEE CNF

- ☐ **21. Behavioral synthesis for hierarchical testability of controller/data path ci
conditional branches**
Bhatia, S.; Jha, N.K.;
Computer Design: VLSI in Computers and Processors, 1994. ICCD '94. Proce
International Conference on
10-12 Oct. 1994 Page(s):91 - 96
Digital Object Identifier 10.1109/ICCD.1994.331862

[AbstractPlus](#) | Full Text: [PDF\(552 KB\)](#) IEEE CNF

- ☐ **22. A behavioral synthesis system for asynchronous circuits**
Sacker, M.; Brown, A.D.; Rushton, A.J.; Wilson, P.R.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 12, Issue 9, Sept. 2004 Page(s):978 - 994
Digital Object Identifier 10.1109/TVLSI.2004.832944

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(872 KB\)](#) IEEE JNL

- ☐ **23. Behavioral synthesis of analog systems using two-layered design space**
Doboli, A.; Nunez-Aldana, A.; Dhanwada, N.; Ganesan, S.; Vemuri, R.;
Design Automation Conference, 1999. Proceedings. 36th
21-25 June 1999 Page(s):951 - 957
Digital Object Identifier 10.1109/DAC.1999.782234

[AbstractPlus](#) | Full Text: [PDF\(788 KB\)](#) IEEE CNF

- ☐ **24. An intermediate representation for behavioral synthesis**
Dutt, N.; Hadley, T.; Gajski, D.D.;
Design Automation Conference, 1990. Proceedings. 27th ACM/IEEE
24-28 June 1990 Page(s):14 - 19
Digital Object Identifier 10.1109/DAC.1990.114821

[AbstractPlus](#) | Full Text: [PDF\(496 KB\)](#) IEEE CNF

- ☐ **25. Genesis: a behavioral synthesis system for hierarchical testability**
Bhatia, S.; Jha, N.K.;
European Design and Test Conference, 1994. EDAC, The European Conferer
Automation. ETC European Test Conference. EUROASIC, The European Eve
Design, Proceedings.
28 Feb.-3 March 1994 Page(s):272 - 276
Digital Object Identifier 10.1109/EDTC.1994.326865

[AbstractPlus](#) | Full Text: [PDF\(476 KB\)](#) IEEE CNF

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L7	14	(hardware with software with (co-verification coverage)).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L8 L9	3 884	("6321366" "6810442" "6754763").pn. (Swoboda).in.	USPAT US-PGPUB; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR OR	OFF OFF	2005/11/28 16:39 2005/11/28 16:39
L10	29	(profit).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L11	29	"703".clas. and L9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L12	2	"716".clas. and L9	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L13	18	(FPGA PLD (reconfigurable with logic) and (DMA) and (testbench))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L14	158	(EDA) and DMA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L15	10	("5493723" "6356862" "6223272" "6223144" "5329471" "5546562" "6263302" "6188975" "6332201" "6032268").pn.	USPAT US-PGPUB; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39

L16	4	("5911059" "6173419").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L17	8	("5663900" "6161199" "6347395" "6009270" "6185522" "6223144" "6173419" "6516428").pn.	USPAT	OR	OFF	2005/11/28 16:39
L18	5	("6202044" "5748875" "5978584" "6356862" "6718294").pn.	USPAT	OR	OFF	2005/11/28 16:39
L19	3	("5748875" "6202044" "5493723").pn.	USPAT	OR	OFF	2005/11/28 16:39
L20	0	(EDA) same (internal with bus) with (PLA PLD FPGA MCM))	USPAT	OR	OFF	2005/11/28 16:39
L21	27	(EDA) with (PLA PLD FPGA MCM)	USPAT	OR	OFF	2005/11/28 16:39
L22	0	"09/954715"	USPAT	OR	OFF	2005/11/28 16:39
L23	0	"09/954715"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L24	1	"09918600"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L25	0	EDA same PCI same DMA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L26	14	EDA same PCI	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L27	115	(hardware with software with (co-simulation co-simulation))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39

L28	78	(hardware with software with (co-verification coverage)))	US-PGPUB; USPAT; USOCR; EPO, JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L29	2	"6009256".pn.	US-PGPUB; USPAT; USOCR; EPO, JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L30	128	("3106698" "3287702" "3287703" "3473160" "4020469" "4306286" "4386403" "4488354" "4503386" "4541071" "4577276" "4578761" "4593363" "4612618" "4621339" "4642487" "4656580" "4656592" "4675832" "4682440" "4695999" "4697241" "4700187" "4706216" "4736338" "4740919" "4744084" "4747102" "4752887" "4758985" "4768196" "4777606" "4786904" "4787061" "4791602" "4803636" "4811214" "4815003" "4823276" "4827427" "4835705" "4849904" "4849928" "4862347" "4870302" "4872125" "4876466" "4882690" "4901259" "4901260" "4908772" "4914612" "4918440" "4918594" "4922432" "4924429" "4931946" "4935734" "4942536" "4942615" "4945503" "4949275" "4951220" "4965739" "5003487" "5023775" "5036473" "5041986" "5046017" "5051938" "5053980" "5081602" "5084824" "5093920" "5109353" "5114353" "5126966" "5128871" "5140526" "5146460" "5189628" "5193068" "5197016" "5224056" "5231588" "5231589" "5233539" "5253181" "5258932" "5259006" "5260881" "5263149" "5272651" "5329470" "5343406" "5352123" "5371390" "5377124" "5425036" "5448496" "5448522" "5452227" "5452231" "5452239" "5467462" "5475830" "5477475" "5504354" "5563829" "5612891" "5644515" "5649167" "5649176" "5654564" "5657241" "5659716" "5661409" "5661662" "5761097" "5796623" "5841967" "5867541" "6009256" "6009531".PN.	OR	OFF	2005/11/28 16:39	

L31	20	(US-5937179-\$ or US-5684721-\$ or US-5329471-\$ or US-6691268-\$ or US-6836877-\$ or US-5546562-\$ or US-6356862-\$ or US-6223144-\$ or US-6188975-\$ or US-5663900-\$ or US-6202044-\$ or US-6286114-\$ or US-6182247-\$ or US-6212489-\$ or US-6052524-\$ or US-6075935-\$ or US-6209120-\$).did. or (US-6212489-\$ or US-6188975-\$ or US-6009256-\$). did.	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L32	11	L31 and (eda and model and bus (reconfig\$ FPGA PLD) and memory)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L33	1	L32 and DMA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L34	4	L31 and DMA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L35	1	L32 and (shared adj memory)	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L36	2	L31 and (eda and model and bus and (reconfig\$ FPGA PLD) and memory)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L37	9	L31 not L32	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L38	1	(behavioral with (RTL gate)).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L39	33	(behavioral with synthesis\$).ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39

L40	0	"7564951".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L41	2	"5764951".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L42	8	("4827427" "5111413" "5128871" "5237513" "5274793" "5437037" "5544066" "5572437").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L43	31	("4353117" "4587625" "4635208" "4675832" "4697241" "4703435" "4789944" "4805113" "4813013" "4827427" "4831543" "4833619" "4890238" "4908772" "4918614" "4922432" "4965741" "4967367" "4970664" "5005136" "5034899" "5084824" "5111413" "5164908" "5164911" "5220512" "5222030" "T940008" "T940020").pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L44	11	eda and ((sharp3 adj3 memory) with (co-simulation co-simulation co-verification co-verification))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L45	11	eda and (((sharp3 common central host) adj3 memory) with (co-simulation co-simulation co-verification co-verification))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L46	11	eda and (((sharp3 common central target) adj3 memory) with (co-simulation co-simulation co-verification co-verification))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L47	0	(hardware with design with tool) and (((sharp3 common central target) adj3 memory) with (co-simulation co-simulation co-verification co-verification))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L48	10	(design with tool) and (((sharp3 common central target) adj3 memory) with (co-simulation co-simulation co-verification co-verification))	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39

L49	136	((shared common host joint target) with memory) and (hardware with software) and (co-verification co-simulation)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L50	2	"5838948".pn.	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L51	80	eda and control\$4 and DMA	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L52	3	("5815688" "5838948" "6134516").pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L53	34	("4835736" "5058114" "5568437" "5572712" "5640542" "5717699" "5764079" "5821771" "5870410" "5960191" "6014334" "6016563" "6020758" "6157210" "6182247").pn. OR ("6286114").ORPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L54	0	(FPGA PLD (reconfigurable adj logic)) same memory same (hardware with software) same (cosimulation co-simulation\$6)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L55	0	(FPGA PLD PLA) same memory same (hardware with software) same (cosimulation co-simulation\$6)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L56	1302	(FPGA PLD PLA) same memory same (hardware with software)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L57	179	(FPGA PLD PLA) with memory with (hardware with software)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L58	8	("5889565" "6370675" "6083269" "5838947").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L59	4	("5889565" "6370675" "6083269" "5838947").pn.	USPAT	OR	OFF	2005/11/28 16:39

L60	140	quidktum.as.	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L61	0	L60 and DMA	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L62	0	L60 and (direct with memory with access)	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L63	4	L60 and (shared with memory)	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
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L72	15	L71 and ((share\$4 with memory) and DMA)	USPAT	OR	OFF	2005/11/28 16:39
L73	3	("5197130" "5784630" "6167502"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39

L74	180	("3106698" "3287702" "3287703" "3473160" "3810577" "3928730" "3955180" "4020469" "4032899" "4306286" "4315315" "4357678" "4386403" "4404635" "4459694" "4488354" "4503386" "4510602" "4524240" "4525789" "4527115" "4527249" "4539564" "4541071" "4577276" "4578761" "4583169" "4587625" "4593363" "4600846" "4612618" "4613940" "4621339" "4642487" "4656580" "4656592" "4674089" "4675832" "4695740" "4695999" "4697241" "4700187" "4706216" "4713557" "4722084" "4725835" "4725971" "4736338" "4740919" "4744084" "4747102" "4752887" "4758745" "4758985" "4761768" "4766569" "4768196" "4769817" "4777606" "4782440" "4782461" "4786904" "4787061" "4787062" "4791602" "4803636" "4811214" "4815003" "4819150" "4823276" "4827427" "4829202" "4835705" "4845633" "4849904" "4849928" "4854039" "4855669" "4862347" "4864165" "4868419" "4870302" "4873459" "4876466" "4879646" "4882690" "4899273" "4901259" "4901260" "4908772" "4914612" "4918440" "4918594" "4922432" "4924429" "4931946" "4935734" "4937827" "4942536" "4942615" "4945503" "4949275" "4951220" "4958324" "4965739" "4972334" "4972372" "5003487" "5023775" "5031129" "5036473" "5041986" "5046017" "5051938" "5053980" "5068812" "5081602" "5083083" "5084824" "5093920" "5109353" "5114353" "5126966").PN. OR ("5128871" "5140526" "5172011" "5224055" "5224056" "5231588" "5231589" "5233539" "5253363" "5259006" "5276854" "5321828" "5329470" "5329471" "5331571" "5339262" "5341483" "5345580" "5352123" "5377123" "5386550" "5396498" "5425036" "5437037" "5448496" "5448522" "5452231" "5452239" "5475624" "5475830" "5477475" "5479355" "5530958" "5544069" "5546562" "5551013" "5563829" "5572710" "5574388" "5596742" "5612891" "5623664" "5649176" "5659716").PN. OR ("5970240").UR.PN	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
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L75	2	09/900124	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L76	908	(DMA with PCI) and (emulat\$4 simulat\$4 model\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L77	39	(DMA with PCI with (reconfig\$6 FPGA PLD PLA MCM)) and (emulat\$4 simulat\$4 model\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L78	187	(DMA with (reconfig\$6 FPGA PLD PLA MCM)) and (emulat\$4 simulat\$4 model\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L79	148	L78 not L77	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L80	1	"6321366".pn.	USPAT	OR	OFF	2005/11/28 16:39
L81	1	US20020152060\$A	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L82	4	("5838948" "5815688").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L83	1	"5450551".pn.	USPAT	OR	OFF	2005/11/28 16:39

L84	28	(US-5937179-\$ or US-5684721-\$ or US-5329471-\$ or US-6691268-\$ or US-6836877-\$ or US-5546562-\$ or US-6356862-\$ or US-6223144-\$ or US-6188975-\$ or US-5663900-\$ or US-6202044-\$ or US-6286114-\$ or US-6182247-\$ or US-6212489-\$ or US-6052524-\$ or US-6075935-\$ or US-6209120-\$ or US-5572437-\$ or US-6298320-\$ or US-6108494-\$ or US-5838948-\$ or US-5815688-\$ or US-5968161-\$ or US-5661662-\$ or US-5970240-\$ or US-6094532-\$).did. or (US-6286128-\$ or EP-453171-\$). did.	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L85	9	L84 and (plural\$5 and reconfig\$8)	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L86	1174	FPGA with interconnect\$4	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L87	10	L86 and (hyper-cube hypercube)	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L88	141	series adj FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L89	0	(series adj interconnect\$4) with FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L90	27	(series with interconnect\$4) with FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L91	29	daisy with chain with FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L92	171	703/20.ocds.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39

L93	2125	719/312,313,318,319,310.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L94	4	L93 and unix and (verilog vhdl (hardware adj descript\$6 adj language))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L95	10	L93 and (verilog vhdl (hardware adj descript\$6 adj language)) and (simulat\$4 emulat\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L96	17	L93 and (verilog vhdl (hardware adj descript\$6 adj language))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L97	355	L93 and (simulat\$4 emulat\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L98	2	"5109353".jrn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L99	10	software with hardware with pointer with mapping	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L100	1243	hardware with software with mapp\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39

L101	380	L100 and pointer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L102	370	L101 not L99	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L103	41	(control with logic) and ((data-in with pointer with logic) or (data-in with latch with logic))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L104	10	(control with logic) and ((data-in with pointer with logic))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L105	5	(pointer with based) same (hardware with software with mapping)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L106	19	(pointer) same (hardware with software with mapping)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L107	28	(US-5937179-\$ or US-5684721-\$ or US-5329471-\$ or US-6691268-\$ or US-6836877-\$ or US-5546562-\$ or US-6356862-\$ or US-6223144-\$ or US-6188975-\$ or US-5663900-\$ or US-6202044-\$ or US-6286114-\$ or US-6182247-\$ or US-6212489-\$ or US-6052524-\$ or US-6075935-\$ or US-6209120-\$ or US-5572437-\$ or US-6298320-\$ or US-6108494-\$ or US-5838948-\$ or US-5815688-\$ or US-5968161-\$ or US-5661662-\$ or US-5970240-\$ or US-6094532-\$).did. or (US-6286128-\$ or EP-453171-\$). did.	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L108	6	L107 and pointer	USPAT; DERWENT	OR	OFF	2005/11/28 16:39

L109	229	hardware with software with pointer	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L110	18	L109 with (simulat\$4 emulate\$4 model\$6)	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L111	1	"5867541".pn.	USPAT	OR	OFF	2005/11/28 16:39
L112	4	("5649176" "5659716" "5761097" "609531").pn.	USPAT	OR	OFF	2005/11/28 16:39
L113	1139	delay with insensitive	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L114	519	delay adj3 insensitive	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L115	64	(delay adj3 insensitive) with asynchronous	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L116	42	(timing with insensitive) same (trigger latch)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L117	517	(timing with insensitive)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L118	19	L117 and ((glitch adj2 free) or glitchless)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L119	554	(glitch near free) and (trigger or latch or flip\$flop)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L120	566	(glitch with free) and (trigger or latch or flip\$flop)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L121	228	(glitch with free) same (trigger or latch or flip\$flop)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L122	12	((gated or derived) near clock) same ((glitch adj less) or glitchfree or (glitch adj free) or glitchless)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L123	10	FPGA same (external adj I/O) same simulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L124	10	reconfig\$6 :same (external adj I/O) same simulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39

L125	10	(PLA PLD FPGA MCM) same (external adj I/O) same simulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L126	0	(PLA PLD FPGA MCM) same (external adj device) same simulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L127	0	FPGA same (external adj device) same simulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L128	0	FPGA same (external adj device) same (simulat\$4 emulate\$4 model\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L129	10	FPGA same (external adj I/O) same (emulat\$4 model\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L130	50	FPGA same (external adj I/O)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L131	40	L130 not L124	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L132	146	(external with I/O) with (simulat\$4 emulate\$4 model\$4)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39

L133	136	L132 not L130	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L134	1	read write multiple FPGA	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	OFF	2005/11/28 16:39
L135	0	(multiple with FPGA) same (access interface I/O read write)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	OFF	2005/11/28 16:39
L136	307	(multiple with FPGA) same (access interface I/O read write)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L137	13	("5497498" "5535342" "5539330" "5583749" "5603043" "5628028" "5784636" "5788669" "5794062" "5981822" "5999990" "6185484" "6230307").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L138	22	bus with selector with FPGA	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L139	196	bus with selector and FPGA	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L140	195	703/28.cds.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L141	357	703/21.cds.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L142	21	L141 and FPGA	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L143	560	703/26,19.cds.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L144	74	L143 and (FPGA reconfig\$6 PLA PLD MCM)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39

L145	40	(US-6169422-\$ or US-5387825-\$ or US-5808486-\$ or US-5539330-\$ or US-5109353-\$ or US-5329471-\$ or US-5363501-\$ or US-5546562-\$ or US-5572437-\$ or US-5661662-\$ or US-5663900-\$ or US-5684721-\$ or US-5815688-\$ or US-5838948-\$ or US-5905883-\$ or US-5911059-\$ or US-5937179-\$ or US-5968161-\$ or US-5970240-\$ or US-6052524-\$ or US-6075935-\$ or US-6094532-\$ or US-6108494-\$ or US-6182247-\$ or US-6188975-\$ or US-6202044-\$).did, or (US-6209120-\$ or US-6212489-\$ or US-6223144-\$ or US-6286114-\$ or US-6298320-\$ or US-6356862-\$ or US-6691268-\$ or US-6766284-\$ or US-6836877-\$ or US-5535342-\$ or US-5603043-\$ or US-6304903-\$).did, or (EP-453171-\$ or US-6286128-\$).did.	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L146	40	(US-6169422-\$ or US-5387825-\$ or US-5808486-\$ or US-5539330-\$ or US-5109353-\$ or US-5329471-\$ or US-5363501-\$ or US-5546562-\$ or US-5572437-\$ or US-5661662-\$ or US-5663900-\$ or US-5684721-\$ or US-5815688-\$ or US-5838948-\$ or US-5905883-\$ or US-5911059-\$ or US-5937179-\$ or US-5968161-\$ or US-5970240-\$ or US-6052524-\$ or US-6075935-\$ or US-6094532-\$ or US-6108494-\$ or US-6182247-\$ or US-6188975-\$ or US-6202044-\$).did, or (US-6209120-\$ or US-6212489-\$ or US-6223144-\$ or US-6286114-\$ or US-6298320-\$ or US-6356862-\$ or US-6691268-\$ or US-6766284-\$ or US-6836877-\$ or US-5535342-\$ or US-5603043-\$ or US-6304903-\$).did, or (EP-453171-\$ or US-6286128-\$).did.	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L147	21	L146 and (behavior\$3)	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L148	27	L146 and (condition\$4 "if-then")	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L149	27	L146 and (condition\$4 "if-then")	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L150	2	L146 and ("if-then")	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L151	140	("if-then") and (emulat\$4)	USPAT; DERWENT	OR	OFF	2005/11/28 16:39

L152	6821	((emulat\$4 hardware) with interrupt\$4) and ((software simulat\$4))	USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L153	5175	((emulat\$4 hardware) with interrupt\$4) and ((software simulat\$4) with interrupt\$4)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L154	957	((emulat\$4 simulat\$4) and (hardware with interrupt\$5 with software))	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L155	12	((emulat\$4 simulat\$4) and (hardware with initiated with interrupt\$5 with software))	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L156	6	"if-then"\$ with interrupt\$6	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L157	3	"09/918600"	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L158	94	(PLD FPGA PLA reconfig\$9) with hardware with interrupt\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L159	18	("3891974" "5274831" "5511217" "5884023" "5960191" "6055649" "6075941" "6085336" "6173386" "6289300" "6370606" "6385742" "6385747" "6446221" "6522985" "6564339" "6567933" "6681341"). PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L160	2814	emulat\$ with (interrupt\$6 condition\$4)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L161	319	L160 and (FPGA PLA PLD)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L162	3	emulat\$ with (interrupt\$6) with ("test-bench" testbench)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39

L163	3	emulat\$ with (interrupt\$6) with ("test-rig" simulator)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L164	15	emulat\$ with (interrupt\$6) with (suspend wait resume)	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L165	7	("5103394" "5666519" "5678028" "5737579" "5761477" "5815688" "6047381").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L166	9	("4638423" "5077657" "5459872" "5493672" "5546562" "5551013" "5572710" "5574927" "5600579").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L167	12	(hardware with interrupt near software) same emulat\$4	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L168	3	("5737516" "5828824" "6324684").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L169	1627	FPGA and debug\$5	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L170	202	FPGA with debug\$5	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L171	78	(hardware with software with (co-verification coverage))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L172	115	(hardware with software with (co-simulation cosimulation))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L173	175	L171 or L172	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L174	18	L171 and L172	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39

L175	87	L173 and interrupt	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L176	35	(emulat\$4 simulat\$4) and ((hardware with breakpoint\$5) near software)	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L177	2	hardware near interrupt\$4 near service near software	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L178	0	hardware adj interrupt\$4 adj service adj software	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L179	301	hardware with interrupt\$4 with service with software	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L180	0	("2004/0086150").URPN.	USPAT	OR	OFF	2005/11/28 16:39

L181	47	(US-20040086150-\$).did. or (US-5109353-\$ or US-5329471-\$ or US-5363501-\$ or US-5387825-\$ or US-5535342-\$ or US-5539330-\$ or US-5546562-\$ or US-5572437-\$ or US-5603043-\$ or US-5661662-\$ or US-5663900-\$ or US-5684721-\$ or US-5808486-\$ or US-5815688-\$ or US-5838948-\$ or US-5905883-\$ or US-5911059-\$ or US-5937179-\$ or US-5968161-\$ or US-5970240-\$ or US-6052524-\$ or US-6075935-\$ or US-6094532-\$ or US-6108494-\$ or US-6169422-\$ or US-6182247-\$).did. or (US-6188975-\$ or US-6202044-\$ or US-6209120-\$ or US-6212489-\$ or US-6223144-\$ or US-6286114-\$ or US-6298320-\$ or US-6304903-\$ or US-6356862-\$ or US-6691268-\$ or US-6766284-\$ or US-6836877-\$ or US-5600579-\$ or US-5870588-\$ or US-5937185-\$ or US-3891974-\$ or US-5594890-\$ or US-6057706-\$).did. or (EP-453171-\$ or US-6286128-\$).	US-PGPUB; USPAT; DERWENT	OR	OFF	2005/11/28 16:39
L182	26	L181 and interrupt	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L183	308	hardware with behavior with process\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L184	126	L183 and emulat\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L185	2	"if-then-else"\$ with interrupt\$6	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L186	17	"if-then-else"\$ with hardware	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39

L187	1	"if-then-else"\$ with emulat\$	US-PGPUB; USPAT; USOCR; DERWENT; IBM_TDB	OR	ON	2005/11/28 16:39
L188	43	("4638423" "5077657" "5459872" "5493672" "5546562" "5551013" "5572710" "5574927" "5600579"). PN. OR ("5838948").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L189	1	"5815688".pn.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L190	552	(FPGA hardware) with implement\$ with interrupt	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/28 16:39
L191	42	bunza.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L192	7	bunza.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/11/28 16:39
L193	7	(US-20040038150-\$.dtd. or (US-6188975-\$. or US-5870588-\$. or US-5937185-\$. or US-3891974-\$. or US-5594890-\$. or US-6057706-\$.dtd.	US-PGPUB; USPAT	OR	OFF	2005/11/28 16:39